The Future of Lithography: SEMATECH Litho Forum 2008

C. Grant Willson[†,*] and Bernard J. Roman[‡]

[†]Department of Chemical Engineering, The University of Texas at Austin, 1 University Station C0400, Austin, Texas 78712-0231, and [‡]SEMATECH, 2706 Montopolis Drive, Austin, Texas 78741

ABSTRACT **The biannual SEMATECH Litho Forum was held May 12—14, 2008 in Bolton Landing, NY, not far from SEMATECH's facility at Albany Nanotech. This biannual meeting is designed to assess the progress in advanced patterning technology and to produce consensus about the processes that will be used to manufacture the next generations of devices. A summary of the key ideas presented at the meeting is given in this paper, along with the future challenges and opportunities in emerging lithographic technologies.**

SEMATECH is a consortium of major semiconductor manufacturers that sponsors and conducts leading edge research in a variety of areas related to semiconductor manufacturing and supports the famous International Technical Roadmap for Semiconductors (ITRS).[1] SEMATECH also conducts a number of meetings that bring together representatives of the semiconductor manufacturers, tool, and materials suppliers to that industry, and academics, the purpose of which is to assess the status of worldwide development in all areas related to semiconductor manufacturing. Among these is the well-known Litho Forum. This meeting, which is held biannually, is designed to assess progress in advanced patterning technology and to produce some consensus about the processes that will be used to manufacture the next generations of devices. The most recent meeting was held in Bolton Landing, New York, near SEMATECH's facility at Albany Nanotech.

The focus of this meeting was patterning technology for the next generations of semiconductor devices, which are to have minimum features (defined as the metal 1 half-pitch for DRAM and MPU/ASIC devices) of 32 nm (2013), 23 nm (2016), and 16 nm (2019), respectively. The year in parentheses is the scheduled first date of manufacturing release for each generation of these devices according to the ITRS. Developing robust manufacturing processes for such incredibly small and complex structures is a challenge for materials scientists, engineers, and physicists, all of whom were represented at the meeting. There are several alternative approaches to printing features of arbitrary shape at such dimensions. Champions for each approach presented what was surely the most optimistic assessment of their favored approach, and at the end of the symposium, a survey was conducted for the purpose of capturing an assessment of the opinions of the assembled experts in regard to the likelihood of success of each approach and the development schedule for each.

Today, devices with nominal minimum dimensions of 45 nm are in full scale production. These devices, like all before them, are patterned by projection optical lithography. The largest contributor to continued progress in shrinking of microelectronic devices derives from improvements in the resolution of optical lithography, defined by

$$R = k\lambda / \mathrm{NA} \quad (1)$$

The minimum feature (R) that can be resolved by this process is directly proportional to the wavelength of the light (λ) used to project the image of the mask pattern on photoresist and inversely proportional to the numerical aperture (NA) of the projection optics. Each variable in this equation has been attacked in an attempt to lower the resolution limit.

The larger the proportionality constant (k), the less sensitive the imaging process will be to variations in exposure energy and focus. In the 1980s, this factor was ~0.8 for manufacturing processes. Today, it is approaching 0.3; no image is possible below a k value of 0.25. Manufacturers have learned to exercise incredible control over these processes through use of statistical and subsystem process control. For example, the temperature control on current

*Address correspondence to willson@che.utexas.edu.

Published online July 22, 2008.
10.1021/nn800410c CCC: $40.75

© 2008 American Chemical Society

imaging tools is in the range of a few millidegrees and focus control is in the range of a few nanometers.

Over time, exposure wavelengths have been reduced from over 400 nm to the ArF excimer laser radiation at 193 nm used today. Attempts to reduce it to 157 nm consumed huge sums of research and development dollars worldwide before the effort was abandoned because it was not warranted by the increment of improvement derived from the shift in wavelength and because of serious technical challenges created by working with light in the vacuum ultraviolet (UV) spectral region. For example, 157 nm wavelength light is absorbed by water, air, and all simple organic materials, such as polyethylene, and by fused silica, the traditional lens material; these and other challenges simply could not be solved in a timely fashion. There is a large effort in place to employ light in the extreme ultraviolet (EUV) spectral region (11−14 nm). The first full scale prototype EUV exposure tools have been delivered, and their performance is being assessed in the fabrication of integrated test devices. Assuming resolution of many technical challenges and issues involving EUV masks, sources, and resists, the technology offers the potential of extending "traditional" step-and-scan reduction lithography to the 11 nm half-pitch node. This presumed extensibility has continued to drive investment in EUV exposure tool development by the major system integrators as well as EUV infrastructure development by consortia, national laboratories, and many industry suppliers.

The NA of a refracting lens has a limit of 1.0 in air. Early projection tools had NA of 0.16, but today, exposure tools with lenses having NA greater than 0.95 have been produced. By introducing high refractive index liquids into the gap between the final lens element and the wafer surface, it is possible to build lenses with NA greater that 1.0. Current so-called immersion lithography manufacturing tools have water in that gap, enabling a maximum NA of ~1.35. Of course, increasing the index of the liquid medium can result in further increases in NA. There is now an ongoing search for new lens materials, high index fluids, and resists that would enable production of imaging systems with lenses having NA as high as 1.8.

Patterning techniques involving exposure by focused high energy electrons are well-developed, and there is an industry based on use of such techniques for making the photomasks used in projection optical lithography. Electron beam lithography is the highest resolution patterning technique available today. It is possible to pattern structures at 10 nm or below using electron beam exposure. Unfortunately, the process is very slow and therefore expensive. It may take 20 h to print a mask by electron beam lithography, but the mask can be printed by optical lithography at a rate of over 100 copies/min. Because of the excellent resolution of electron beam lithography, attempts have been made for many years to write product directly. In the early 1980s, IBM used electron beam lithography in production for a short time.[2] Unfortunately, the productivity was too low and the process was abandoned. Since that time, efforts have been made to design systems based on projection shadow masks and multiple beams in attempts to improve the productivity of electron beam lithography. These multibeam efforts are still ongoing.

Imprint lithography emerged in the late 1990s as a low-cost alternative to high-resolution patterning.[3] This technology employs various forms of embossing and molding to replicate the relief images rapidly in a master mold or template. Compact discs and DVDs are manufactured in this way. Each variation on the theme has certain applications for which it is best suited. The approach that seems to have made the greatest inroads for fabrication of microelectronics is step and flash imprint lithography (SFIL).[4] In this variation, the template is a quartz plate with a relief structure that is used to pattern a low viscosity formulation of photosensitive monomers. The liquid is deposited as very small drops by an inkjet device, and the drop pattern can be tailored to provide more liquid where there is high pattern density and less where the pattern density is lower, which limits the distance that the liquid must flow to fill the pattern. The liquid is polymerized by flood exposure through the rigid, transparent template so that the process can be run at room temperature and at low pressure, which is optimum for precision pattern placement and alignment of the sort required to manufacture semiconductor devices. This process has been included on the ITRS for several years as an alternative patterning technology. The resolution of the process is limited only by the size of the patterns that can be made in the template. SFIL images smaller than 10 nm have been demonstrated in laboratories, and functional devices with 30 nm images have been reported by IBM.[5] There are concerns about the throughput of this technology and about defect and alignment issues, but the resolution and line edge roughness (LER) are state-of-the-art.

The progress in each of these processes was described in a series of presentations over two days.

High Index Immersion Lithography. The approach to increasing the resolution of optical lithography beyond that available by water immersion was one of the most exciting parts of the conference. ASML and Canon both described progress on systems designed around so-called "generation 2" immersion liquids. These are generally saturated hydrocarbons. Decalin is the classical example of such a fluid. It has a refractive index of 1.65 at 193 nm. However, design of an exposure tool with this immersion fluid also requires use of a new transparent material with an index of refraction greater than 1.65 for the final lens element. The most popular material for this use is Lutetium Aluminum Garnet (LuAG), which has a refractive index greater than 2.0 at 193 nm and, in combination with a "generation 3" immersion fluid having a refractive index of 1.9, can enable a lens in principle with a NA of 1.8 and with a minimum resolution of ~27 nm. Progress on both of these high index materials development projects was summarized at the Litho Forum. Schott Lithotec reported that transparency of their latest LuAG samples was within an order of magni-

tude of what is required, but SEMATECH outlined a possible path to generation 3 immersion fluids using high volume percent mixtures of transparent high index nanoparticles such as HfO_2 in water or decalin.

Nikon shocked the Litho Forum attendees when Dr. Soichi Owa announced that Nikon would not pursue development of exposure tools for high index immersion lithography. He explained that the gain in resolution using generation 2 immersion fluids was less than 20% compared to water, the quality of the LuAG available was inadequate for lens applications, and the rate of improvement in the transmission of the material was not keeping pace with expectations. Furthermore, the use of hydrocarbons like decalin is fraught with problems. These include sensitivity to oxygen, which forms a complex that is strongly absorbing at 193 nm, photolability at 193 nm that produces strongly absorbing photoproducts, low surface tension, which limits scan speed and necessitates the redesign of the fluid handling systems on the exposure stage and the fact that, as Dr. Owa put it, "while water extinguishes fires, decalin is a fuel," with a relatively low (57 °C) flash point. The impact of this presentation is likely to cause significant changes in development activity in this area.

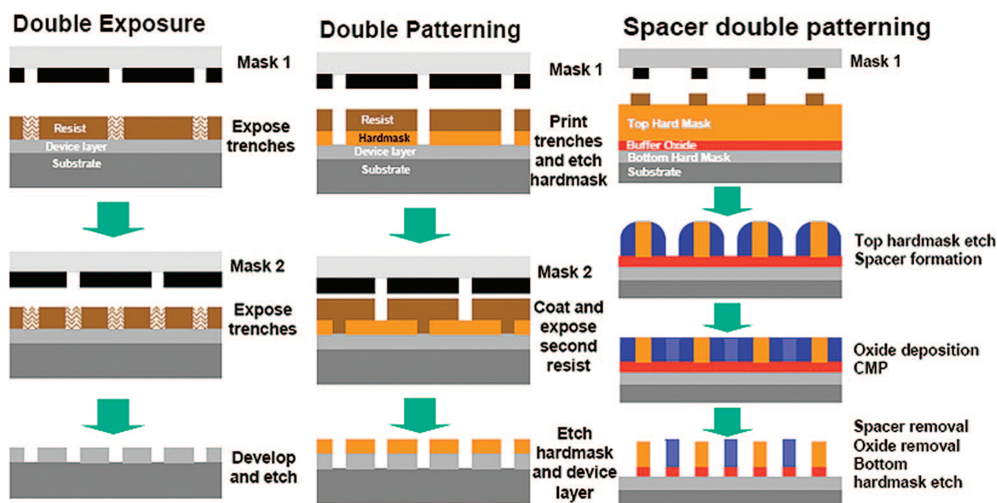

Figure 1. Schematic of double exposure and double patterning process flow. Reproduced with permission from Semiconductor Industry Association. The International Technology Roadmap for Semiconductors, 2007 Edition. SEMATECH: Austin, TX, 2007.

Double Patterning Lithography. Since (a) earlier attempts to increase lithographic resolution by moving to 157 nm (F_2 excimer laser) failed, (b) further NA increases seem unlikely as described above, and (c) we are already operating at the limit of the *k* factor, the remaining alternative to further advances in non-EUV optical lithography depends on "double patterning lithography" (DPL) in some form (Figure 1). This approach involves printing features at the target dimension but at twice the pitch. For example, 30 nm lines are printed with 90 nm spaces. The resist is then developed and the image transferred by etching. The imaged wafer is then recoated with resist and re-exposed with 30 nm lines and 90 nm spaces, aligned so that, after the second etch, they produce a regular grating of 30 nm lines with 30 nm half-pitch. Several papers were presented demonstrating variations on this theme. One of the most impressive of these was presented by Chris Ngai of Applied Materials. He showed the results of a self-aligned double patterning process (SADP) that involves initial imaging at 2× final pitch in an advanced patterning film (APF) (essentially amorphous carbon) followed by deposition of a conformal plasma-enhanced chemical vapor deposition (PECVD) dielectric spacer layer at a thickness approximately equal to the final half-pitch. This layer is then subjected to an anisotropic etch that removes the original deposition thickness, leaving only the material deposited on the side wall of the original APF pattern. Removal of the APF then generates the desired 1× grating in the PECVD material. Applied Materials demonstrated examples of this process down to 22 nm half-pitch, including final pattern transfer into a variety of underlying films. The image quality and LER from their process appeared to be excellent (Figure 2).[6]

The problem with DPL is that it requires twice as many etch tools, twice as many exposure tools, twice as much resist, antireflection and top coat material, and, in some cases, demands a precision and accuracy of mask-to-mask overlay that is a few percent of the target line width or approximately 2−3 nm (mean plus 3-σ)! The exposure system vendors—ASML, Canon, and Nikon—demonstrated alignment of about 5−7 nm, which is certainly impressive, but not yet adequate for all DPL applications. Clearly, the cost of implementing DPL is very high, but at the moment, it seems that some variation on the DPL process is the only viable alternative to printing 32 nm devices, particularly for aggressive NAND Flash applications scheduled for introduction in 2009. This is a welcome realization for the vendors of exposure tools, deposition tools, etchers, and imaging materials!

There is work being done by industrial laboratories and academic institutions on a DPL variation called double exposure lithography (DEL). In the case of 30 nm half-pitch patterning, DEL involves exposing 30 nm lines and 90 nm spaces in two 60 nm offset passes into the same resist layer, followed by resist

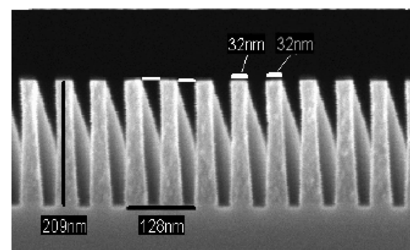

Figure 2. High-aspect-ratio 32 nm patterns produced by Applied Materials Process. Reproduced with permission from ref 6.

development and transfer of the composite image into the substrate (Figure 1). This saves removing the wafer from the chuck of the exposure tool, greatly improving overlay accuracy. In addition, it removes half of the process steps and half of the tools and materials required to pattern each layer. Clearly, this is an attractive alternative. Unfortunately, success in this approach demands a material that does not yet exist—a nonlinear resist, *i.e.*, a "magic material" that can "forget" subthreshold exposure. A research effort that includes Columbia University, The University of Texas, TOK, JSR, Central Glass Co., and Samsung has begun work to identify such a material.

We know of no photosensitive materials that can "forget" that they were subjected to subthreshold exposure. In general, if a photoresist requires 20 mJ/cm^2 to become soluble and is exposed to 10 mJ/cm^2 in a first exposure, it remains insoluble, but then a subsequent exposure requires only an additional 10 mJ/cm^2 to render the film soluble. First-order phase transitions have this ability to forget. For example, if a material is heated to a temperature just below the melt transition (threshold) and then cooled, it has no memory of that heating event. The same number of Joules is required to raise it to the melt temperature as if it had never been heated previously. However, there is not enough energy in 193 nm exposures as tools are currently configured to produce a significant temperature change in the resist, so the research team is designing systems that exploit reversible photoisomerization to change a phase transition temperature reversibly in a polymeric material from slightly above room temperature to below room temperature. To that end, they are testing a series of photochromic systems. Significant technical progress was reported, including exciting proof-of-principle demonstrations, but no imaging results were provided. This work is being supported by SEMATECH and is being watched very closely by the lithography community. It is a high-risk project, with the potential of a high return.

Extreme Ultraviolet Lithography. The EUV exposure option was reviewed in some detail at the Litho Forum, including a report on the first use of the ASML Alpha Demo tool (one of the two in existence) at Albany Nanotech to pattern a critical layer (metal 1) of an active 45 nm technology test device. The pattern quality was acceptable, and the devices had excellent electrical characteristics, but the exposure tool throughput was very slow and there are already 45 nm technology generation devices in full production using optical lithography. ASML and Nikon showed progress in the development of their tools, but there are serious problems that still must be overcome before these tools are ready for wafer manufacturing. The major problem still seems to be the light source. Philips Extreme UV described progress on their light source based on plasma discharge in tin metal vapor. Current Alpha sources are delivering about 20 W of EUV in band power at intermediate focus (IF), still about an order of magnitude below that required for high-volume manufacturing (HVM) tools. Cymer described recent results with their CO_2 laser-produced plasma source yielding 25 W average power at IF for 1.5 h, still also far below HVM requirements. There was demonstration of improvement in resist performance both in terms of LER and resolution, but no images were shown at 22 nm half-pitch, the target critical dimension (CD) regime for HVM using EUV technology. Finally, SEMATECH reported steady progress in producing EUV mask blanks with very low defect densities using ion beam deposition and etchback "defect smoothing" techniques. However, the best defect density demonstrated is still almost 2 orders of magnitude too high, and a 2× improvement in defect detection sensitivity is needed for HVM. Overall, progress in EUV lithography continues, but there are a number of daunting issues that must be resolved before it can be adopted for manufacturing due to cost of ownership issues. Source power as well as resist and mask technology appears to be the biggest issues, but there are also significant engineering challenges associated with maintaining integrity of the projection optics with respect to surface contamination and temperature control, lifetime of source condenser optics, and preservation of a defect-free reticle environment.

Progress in EUV lithography continues, but there are a number of daunting issues that must be resolved before it can be adopted for manufacturing due to cost of ownership issues.

Maskless Lithography. The sessions listed as "maskless lithography" (ML2) were dedicated to high speed, multibeam electron beam writing approaches. Mapper Lithography has a unique approach to achieving parallelism in electron beam exposure. In their system, multiple beams are rastered by a combination of mechanical and electrostatic processes and blanked by a unique application of light signals. Mapper Lithography showed 45 nm images that were high quality, obtained using 110 beams and static exposure, but the throughput of the tool has yet to be demonstrated. It will have to work at much higher current using 13 000 beams to achieve workable throughput for direct wafer exposure. Field stitching also needs to be demonstrated.

IMS Nanofabrication provided an update on their multibeam architecture, an Alpha tool version which is scheduled for completion in 2009. Their tool is based on 200× reduction optics and 40 000 beams created by a clever aperture and blanking plate technology. Images as small as 16 nm were presented using a 2000 beam proof-of-concept test bench, demonstrating the quality of the optics at low beam current.

The good news is that these ML2 machines can have thousands of beams operating in parallel in principle, yielding $<$20 nm resolution at a throughput of 10 wafers/h (WPH) without need for a

mask. The bad news is that each beam requires a data rate approaching 10 Gb/s! This creates a daunting data transfer and storage requirement and has yet to be demonstrated. Progress on multibeam lithography has indeed been impressive, but there is a long way to go to reach a convincing throughput demonstration.

Imprint Lithography. The imprint lithography session was devoted to SFIL. Toshiba and Samsung both presented excellent imaging results with respect to resolution and LER using Molecular Imprints Inc. (MII) imprint tools. Samsung is working with DNP who provided 28 nm half-pitch templates written with a shaped-beam mask writer. This is an encouraging result because the write time for the templates was ~10 h and is therefore comparable to the write time required for today's advanced optical masks. Toshiba reported 22 nm patterning with Hoya templates, but these were written with a slower Gaussian beam exposure system. Both companies reported excellent CD uniformity and LER data, with mix-and-match overlay to 193 nm scanners in the range of 20−35 nm. The defect data that were presented also demonstrated improvement. MII reported current imprint mask defect density to be $<0.1/cm^2$ and imprint-related wafer defect density to be $<1/cm^2$. Issues still remain with 1× template inspection, particularly with charging effects associated with electron beam inspection, and with tool throughput. MII presented a roadmap to improved overlay and to a 20 wafer/h throughput, but even that throughput is 5× slower than current optical systems. It is unclear whether SFIL tools can be improved at a rate that will intersect the ITRS at 22 nm, but there seem to be no fundamental issues limiting progress. An MII tool will be delivered to SEMATECH at Albany Nanotech in the next 2 months, which will help clarify the outlook for the viability of this technology.

Panel Discussion. A panel discussion was held after the presentations. The members of the panel included representatives from IBM, Intel, Freescale, TSMC, and MII. There was a spirited discussion of the technology and business issues that included many questions from the audience. One of the highlights of this discussion was speculation about how the industry will find the support for parallel approaches to high-resolution patterning. The EUV program is perceived to be the recipient of the bulk of research and development dollars, and the alternative technologies (high-index immersion, imprint and maskless programs) voiced concern about some redistribution of resources. Although there was no consensus on resolution of this issue, a possible option includes more partnering among suppliers to leverage core competencies. For example, SFIL tool development might be accelerated through partnership with a precision stage supplier, while ML2 tool development may benefit from partnership of a multibeam column supplier with an exposure tool system integrator. As was pointed out by Multibeam Systems in their Litho Forum presentation, the latter approach is in fact their stated strategy to deliver ML2 tools that are optimized for specific wafer or mask writing applications.

> One of the highlights of the panel discussion was speculation about how the industry will find the support for parallel approaches to high-resolution patterning.

Survey Results. As with previous Litho Forums, surveys on lithography preferences and technology assessment were conducted both prior to the Litho Forum and at its conclusion and provided an interesting look at the expectations and opinions of the technical leaders of the lithography community. The pre-Forum survey was directed only to lithography end-users, that is, integrated device manufacturers (IDMs) and foundry chip manufacturers as well as major consortia, with care also taken to ensure that responses reflected reasonably the industry's geographic and revenue makeup. The post-Forum survey captured responses from all Litho Forum attendees, which historically has included a large percentage of suppliers. In general, responses from end-users were quite consistent in both surveys and were therefore combined, whereas responses from suppliers and other participants were reported separately.

Perhaps the most closely watched survey result is the lithography technology preference by year, as measured by the percentage of responses to the question, "What lithography technology will your company likely employ or support in 2010, 2013, and 2016 for gate manufacturing in leading edge products, assuming all technologies are available?" Pre- and post-Forum survey responses to this question were combined with a similar question related to contact manufacturing and are shown in Figure 3. Not surprisingly, 193 nm immersion (single exposure) and 193 nm dry or immersion (double patterning)

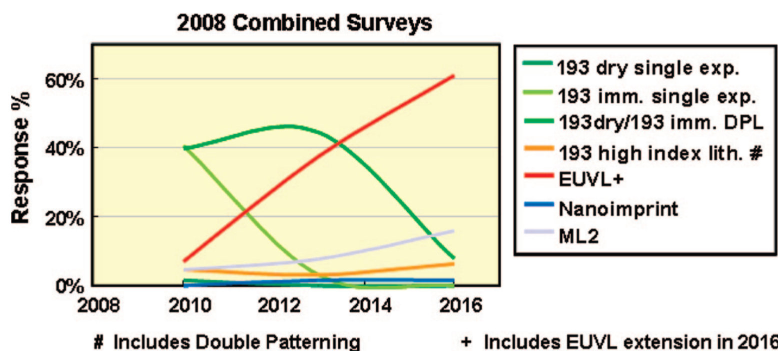

Figure 3. Combined pre- and post-2008 Litho Forum survey responses on lithography technology preferences for gate and contact patterning to be used on leading-edge products. Responses were only from end-users: integrated device manufacturers, foundries, and consortia.

are the overwhelming preferences in 2010 due to alignment of lithography capabilities and requirements in that year. Somewhat surprising is that 193 nm dry or immersion DPL remains the primary choice in 2013 when leading edge products at or below 32 nm half-pitch are in manufacture according to the ITRS as well as 2008 survey responses. However, EUV lithography is also expected to have a significant presence in 2013 and is clearly the overwhelming preference in 2016 for nominal 22 nm half-pitch manufacturing requirements, particularly if technology extensions (*i.e.*, higher NA EUV lithography systems) are also considered. A smaller, but still significant, demand appears to be developing for maskless lithography, especially in 2016 where its response is about 25% compared to that for EUV lithography. Overall, the industry appears to be accepting the cost and process complexity issues of DPL in the short run, is assuming that EUV lithography manufacturing issues will be overcome in the long run, but is also looking longer term at an alternative technology, at least for some applications.

CONCLUSIONS AND PROSPECTS

There was a great deal of "hallway discussion" about the future of patterning technology and of the semiconductor industry. The industry is approaching physical limits in several areas: there can be no further improvement in *k*, the wavelength of "optical exposure" will not go below 193 nm and significant further increases in NA are problematic. Therefore, further improvement in resolution of optical imaging will be achieved by dramatic increases in process complexity and higher materials and equipment costs. Introduction of new imaging technology such as EUV, ML2, and SFIL shows promise, but intersection with ITRS requires an increase in the pace of development and clearly demands more investment of research and development dollars. DARPA, who played a very significant (and at times, critical) role in all lithography developments to date, has chosen to support electron beam exposure development in the U.S. The new European MAGIC consortium is also in place to support validation of multibeam technology for 32 nm half-pitch applications by the end of 2010. The EUV programs at SEMATECH, the European Union, and Japan are well funded and making progress. To date, SFIL is not being supported at these same levels.

Perhaps we will be wed, as many have predicted, to optical imaging forever, with all other candidate technologies disappearing from the ITRS in the same way as scattering with angular limitation projection electron beam lithography (SCALPEL), 157 nm exposure, shadow X-ray, and so many other "next generation lithography" approaches have done in the past. Or, perhaps one of these technologies will successfully carry the industry into the place where physical limits in other aspects of the technology besides lithography will limit the rate of progress.

Conflict of interest: C.G.W. declares that he has founded Molecular Imprints Inc., an imprint nanolithography company (and currently is Chairman of its Technical Advisory Board).

REFERENCES AND NOTES

1. http://www.itrs.net/.
2. Pfeiffer, H. C. Direct Write Electron Beam Lithography—A Production Line Reality. *Solid State Technol.* **1984**, 223–227.
3. Chou, S. Y.; Krauss, P. R.; Zhang, W.; Guo, L.; Zhuang, L. Sub-10 nm Imprint Lithography and Applications. *J. Vac. Sci. Technol. B* **1997**, *15*, 2897–2904.
4. Colburn, M.; Johnson, S.; Damle, S.; Bailey, T.; Choi, B.; Wedlake, M.; Michaelson, T.; Sreenivasan, S. V.; Ekerdt, J.; Willson, C. G. Step and Flash Imprint Lithography: A New Approach to High-Resolution Patterning. *Proc. SPIE* **1999**, *3676*, 379–389.
5. Hart, M. W. Step and Flash Imprint Lithography for Storage-Class Memory Presented at the EIPBN June 2007 and IEEE Lithography Workshop; December 2007, http://www.molecularimprints.com/NewsEvents/tech_articles/new_articles/EIPBN2007_IBMv2.pdf.
6. Borst, C. L; Montgomery, W.; Huli, L.; Brookhart, D.; Bennett, S.; Rodgers, M.; Piccirillo, J.; Dai, H.; Ngai, C.; Bencher, C.; *et al.* Driving Metallization Dimension to Sub-30 nm Using Immersion Lithography and a Self-Aligned Double Patterning Scheme. In *Advanced Metallization Conference (AMC2007)*, 2007; McKerrow, A. J. , Shacham-Diamand, Y. , Shingubara, S. , Shimogaki, Y. , Eds.; Materials Research Society: Warrendale, PA, 2007.